REMARKS

The claims are claims 1, 2, 5, 6, 9 and 10.

The application has been amended at many locations to correct minor errors and to present uniform language throughout.

Claims 1, 2, 5, 6, 9 and 10 are amended. Claims 3, 4, 7 and 8 are cancelled. Claim 1 has been amended in response to the rejection under 35 U.S.C. 112. Claims 1, 2 and 6 have been amended to change "close data processing cores" to "data processing cores having said close connection" and to change "far data processing cores" to "data processing cores having said far connection." This amended language is believed a better reflection of the antecedence in independent claims 1 and 6. Claims 5 and 9 are amended to further recite that the local memory is not directly connected to the other data processors. Claim 10 is amended to further define the subject matter.

Claim 1 was rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The Examiner states that there is insufficient antecedent basis for the limitation "said close portion" and that "aid" in line 20 should be changed to "said".

Claim 1 has been amended to cure the indefiniteness. As amended, the previous limitation "said close portion of said unified memory" has been changed to "said memory forming said local portion of said unified memory." The Applicant respectfully submits that this amended language finds antecedent basis in the recitations of original line 6 and current line 5. The recitation of "aid" has been changed to "said" as requested by the Examiner.

Claims 1, 2, 5, 6, 9 and 10 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Buktenica et al. (U.S. Patent No. 5,669,009) and Hofmann et al. (U.S. Patent No. 6,513,089).

Claim 1 recites subject matter not made obvious by the combination of Buktenica et al and Hoffman et al. Claim 1 recites "said global memory arbitration logic having a close connection to said data processing core of said corresponding data processor and to said data processing core of at least one other data processor but less than all other data processors and a far connection to said data processing core of additional data processors, said global memory arbitration logic arbitrating access to said memory forming said local portion of said unified memory granting a first type access to said data processing cores having said close connection and a second type access different from said first type access to said data processing cores having said far connection." This portion of claim 1 recites two differing types of connections. The data processing core of the present data processor and that of at least one other data processor have a close connection. The data processing cores of other data processors have a far connection. This portion of claim 1 recites differing types of access based upon these differing types of connections. A close connection may be granted a first type access and a far connection may be granted a second type access.

The combination of Buktenica et al and Hoffmann et al do not make obvious this difference in connection resulting in a difference in kind of access. A second processor of dual processor 11 cannot be "said data processing core of at least one other data processor." Any such second processor of dual processor 11 must be of the same data processor because it does not have a corresponding memory and global arbitration logic as required by claim 1. Dual processor 11 of other processing nodes 20 likewise cannot be "said data processing core of at least one other data processor but less than all other data processors" connected to dual port memory 14 via buses 15 and 20 as recited in claim 1. If the dual processor 11 of any processing nodes 20 is connected to dual port memory 14

via busses 15 and 20, then they all are so connected. Figure 1 of Buktenica et al illustrates the same connections between bus 20 and all dual processor 11. Accordingly, this connection is not to less than all of the data processing cores as required by claim 1. The teaching of Hofmann et al adds nothing to make these limitations obvious. Hofmann et al states at column 3, lines 10 to 19:

> "The present invention separates the pending bus request signals, latency timers, and the pending bus priority signal for a read and a write operation. In embodiments of the present invention, a high priority device is granted a read request while the write bus may be granted to another device with a lower read request but a higher priority write request. The embodiments of the present invention allow bursting reads and writes to remain operational by a low priority device when a higher priority device requests the corresponding other bus operation."

This portion of Hofmann et al makes clear that the connection granted is based upon the priority of the request and not on the connection of the requesting data processing core as recited in claim 1. Accordingly, claim 1 is allowable over the combination of Buktenica et al and Hofmann et al.

Claims 1 and 6 recite further subject matter not made obvious by the combination of Buktenica et al and Hofmann et al. Claim 1 recites the global memory arbitration logic "arbitrating access to said memory forming said local portion of said unified memory granting a first type access to said data processing cores having said close connection." Claim 6 similarly recites "said global memory arbitration logic arbitrating access to said first port of said dual port memory among said data processing cores having said close connection thereby providing a first type access." Review of Figure 1 of Buktenica et al reveals that accesses to dual port memory 14 via bus 15 from dual processors 11 or via buses 15 and 20 from other processing nodes 20 do not pass through control logic

23. Thus these accesses cannot be arbitrated by the bus control logic 23 as required by this limitation of claims 1 and 6. Accordingly, claims 1 and 6 not made obvious by the combination of Buktenica et al and Hofmann et al.

Claims 2 and 8 recite subject matter not made obvious by the combination of Buktenica et al and Hofmann et al. Claims 2 and 8 each recite "said global memory arbitration logic arbitrating access to said first port of said dual port memory among said data processing cores having said close connection thereby providing said first type access and arbitrating access to said second port of said dual port memory among said data processing cores having said far connection thereby providing said second type access." Dual port memory 14 illustrated in Figure 1 of Buktenica et al has a first port connected to bus 15 and a second port connected to bus logic control 23. Any accesses via bus 15 are not through bus control logic 23 of Buktenica et al. Thus these accesses are not arbitrated by the global memory arbitration logic as required by claims 2 and 6. Accordingly, claims 2 and 6 are not made obvious by the combination of Buktenica et al and Hofmann et al.

Claim 1, upon which claim 2 depends, and claim 6 include further subject matter not made obvious by the combination of Buktenica et al and Hofmann et al. Claim 1, upon which claim 2 depends, and claim 6 each recite "said global memory arbitration logic having a close connection to said data processing core of said corresponding data processor and to said data processing core of at least one other data processor but less than all other data processors." A second processor of dual processor 11 cannot be "said data processing core of at least one other data processor." Any such second processor of dual processor 11 must be of the same data processor because it does not have a corresponding memory and global arbitration logic as required by claims 1 and 6. Dual processor 11 of other processing nodes 20 likewise cannot be "said

data processing core of at least one other data processor but less than all other data processors" connected to dual port memory 14 via buses 15 and 20 as recited in claims 1 and 6. If the dual processor 11 of any processing nodes 20 is connected to dual port memory 14 via busses 15 and 20, then they all are so connected. Figure 1 of Buktenica et al illustrates the same connections between bus 20 and all dual processor 11. Accordingly, this connection is not to less than all of the data processing cores as required by claims 1 and 6. Thus claims 2 and 6 are not made obvious by the combination of Buktenica et al and Hofmann et al.

Claims 5 and 9 recite subject matter not made obvious by the combination of Buktenica et al and Hofmann et al. Claims 5 and 9 each recite "each of said data processors further includes a local memory connected to said data processing core and directly accessible by said data processing core and neither directly connected to nor directly accessible by said data processing cores of other data processors." Buktenica et al further teaches each processing node 20 includes a local memory 12 connected to dual data processor 11. However, Buktenica et al fails to teach that these local memories 12 are not directly connected to and accessible by dual processor 11 of other processing nodes 20. Figure 1 illustrates each dual processor 11 and each local memory 12 connected to bus 13 in the same manner. If the dual processor 11 of any processing node 20 is connected to its local memory 13, then the dual processors 11 of all other processing nodes 20 are similarly connected. Buktenica et al fails to state that the dual processors 11 of these other processing nodes 20 are not connected to and cannot directly access each local memory 12. Because Figure 1 of Buktenica et al clearly illustrates the same connection between of all dual processors 11 and all local memories 12 to bus 13, Buktenica et al must explicitly recite the negative limitation to make obvious this limitation of claims 5 and 9. Buktenica et al

fails to state this negative limitation. Accordingly, claims 5 and 9 are not made obvious by the combination of Buktenica et al and Hofmann et al.

Claim 10 recites subject matter not made obvious by the combination of Buktenica et al and Hofmann et al. Claim 10 recites "said global memory arbitration logic of each data processor has a close connection to its corresponding data processor and one other data processor and has a far connection to two other data processors." Figure 1 of Buktenica et al does illustrate four processing nodes 20. However, Buktenica et al fails to teach the differing connections of this limitation of claim 10. Figure 1 of Buktenica et al clearly shows that all processing nodes 20 are connected to bus 13 and to buses 17, 18 and 18a in the same manner. Accordingly, Buktenica et al fails to teach the recited differing close and far connections. Note that the OFFICE ACTION fails to state which connections are close connections and which connections are far connections. The Applicant respectfully submits that this failure is because all the connections are the same and cannot be distinguished are required by claim 10. Accordingly, claim 10 is not made obvious by the combination of Buktenica et al and Hofmann et al.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

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